

Abstract of the Disclosure

A regenerative clock repeater comprises an edge
detector and an output driver means to produce the clock
5 signal by recovering its high logical level and low
logical level. The output driver means further comprises
a pull-up and a pull-down circuitry adapted to receive a
pair of control signals. These control signals are
generated by the edge detector to sense the rising edge
10 and falling edge of the clock signal. Inside the edge
detector, a pair of threshold level detectors detect a
high and a low logical level of the clock signal and
inputs the results to a combination of logic gates and a
latch to keep the locations of the signal markers fixed.
15 These fixed-location of control signals trigger the
output driver means to recover the high logical level and
the low logical level of said clock signal.